Modeling ATM Switches for Performance Management

D. Tsaih, S.S. Panwar, L. Tassiulas, P. Sarachik
Polytechnic University, Brooklyn, New York

Abstract

Modeling switches for performance management has somewhat different objectives as compared to modeling for switch design and performance evaluation. While, in general, a larger modeling error is tolerable in performance management, it has to be fast, consistent and handle general traffic inputs and server types.

As a preliminary step to meeting these goals, we are modeling a shared memory ATM Switch. In this model a heterogeneous set of traffic sources is approximated by a set of identical Markov-modulated rate processes. The main purpose of using this model is that we get closed form or fast numerical solutions for packet loss and the delay distribution. This is very important due to the computational complexity and large round-off errors in computation when a large number of heterogeneous burst sources have to be modeled. The performance measures we are then able to obtain for this switch are average delay, delay jitter (95 percentile delay) and loss probability.

Specifically, our approach is based on an approximation of actual input sources by suitable On-Off sources. Actual sources are composed of a superposition of many heterogeneous sources, each source with a different peak rate, load and first two moments of the burst period and silent period. By matching moments of their arrival rate and correlations we can find a set of identical sources with approximately the same statistics as the original sources. We can then find the queue length distribution and delay distribution. Several numerical examples will be presented to illustrate this modeling technique and to validate performance result